USN

First / Second Semester B.E. Degree Examination, December 2011

Basic Electronics

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing at least two from each part.

- 2. Answer all objective type questions only on OMR sheet page 5 of the answer booklet.
- 3. Answer to objective type questions on sheets other than OMR will not be valued.
- PART A Choose the correct answers for the following: 1 (04 Marks) The voltage at which forward current through the diode starts increasing rapidly is A) Saturation voltage B) Breakover voltage C) cut in voltage D) cut off voltage. Dynamic zener resistance is ——— in reverse breakdown condition. A) very high B) high C) zero D) very small Smaller the ripple factor, the output will have higher iii) — components. B) DC A) AC C) Both AC and DC D) Pulse The transformer utilization factor of a bridge type full wave rectifier is iv) A) 0.287 B) 0.812 C) 0.864 D) 0.48 b. Draw the AC equivalent circuit of a diode. (04 Marks) (06 Marks)
 - c. With a circuit diagram, explain the working of a centre tapped FWR.

d. Prove that ripple factor of a HWR is 1.21.

(06 Marks)

2 a. Choose the correct answers for the following:

(04 Marks)

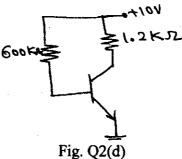
- The current conduction in bipolar junction transistor is because of -A) Electrons
 - B) Holes
- C) Both electrons and holes D) Current
- In cut off region both base to collector and base to emitter junctions are ii)
 - A) forward biased
- B) ON
- C) Reverse biased
- D) None of these
- In a transistor $I_B = 30$ mA and $I_E = 10$ mA. What is the value of α ?
- B) 0.99
- C) 0.98
- D) 0.96
- In CB- mode of a transistor when the reverse bias voltage increases, the width of iv) depletion region also increases, which reduces the electrical base width called as -A) Depletion width B) Early effect
 - C) cut in
- D) punch through effect
- b. What are the advantages of transistor over vacuum tube?

(04 Marks)

c. Draw and explain the input and output characteristics of CE configuration of a transistor.

(06 Marks)

d. For the CE - circuit shown in Fig. 2(d), draw the DC load line and obtain Q-point values. Assume $\beta = 100$ and $V_{BE} = 0.7V$. (06 Marks)



3	a.	Choose the correct answers for the following: i) Ideally stability factor should be zero to get ——— Q-point. A) Unstable B) Centre of the cutoff	(04 Marks)					
		A) Unstable B) Centre of the cutoff C) Stable D) None						
		ii) Which of the following factor affects the Q-point stability? A) I _{CO} B) Coupling capacitor						
		C) Emitter resistor D) Bypass capacitor. iii) In what biasing circuit voltage shunt negative feed back is provided A) Voltage divider biasing B) Fixed bias	1?					
		C) Collector to base bias D) Emitter bias.						
		iv) Fixed bias circuit provides ——— stability						
		A) Poor B) High						
	h	C) Better D) Very good For the circuit shown in Fig. Q3(b), $I_C = 2$ mA, $\beta = 100$, and $V_{CE} = 3V$. C	'alculate R, and Ro					
	υ.	Assume $V_{BE} = 0.6V$.	(08 Marks)					
		V21+0-1-15V	(**************************************					
		RI RC						
		Ro LRE						
		10KV 2 600V						
		Fig. Q3(b)						
	c.	What factors cause instability of a Q-point? Explain it.	(08 Marks)					
4		Observed to a served asserting for the full assets	(0.4 h .f.,l.,)					
4	a.	Choose the correct answers for the following: i) JFET is a ———— device	(04 Marks)					
		,	D) None of these					
		ii) PNPN device is an ———						
		A) UJT B) SCR C) MOSFET	D) BJT					
		iii) The UJT relaxation oscillator is used to generate						
		A) Square wave signal B) Rectangular wave s	signal					
		C) Sine wave signal D) Triggering pulse	•					
		iv) The holding current in SCR is ——— latching current	D) None of these					
	b.	A) More than B) Less than C) Equal to Draw the equivalent circuit of a UJT and mention its applications.	(04 Marks)					
	c.	went a de la deserva						
	d.							
			` ,					
		<u>PART - B</u>						
5	a.	Choose the correct answers for the following:	(04 Marks)					
		i) If the voltage gain of the amplifier is 0.001, what is the value of ga						
		A) - 60 B) - 62 C) 60	D) 100					
		ii) With negative feedback, the bandwidth of an amplifier						
		A) Decreases B) Increases C) Both A & B	D) Constant					

	•	iii) iv)	In oscillator circuit _ A) Voltage series In RC - phase shift	B) Positive	back is used C) Negative on of RC – network	D) Both +ve and -ve produces phase shift of -
			A) 60°	B) 30°	C) 180°.	D) 90°
	b. c.	With Expl	n a neat diagram, expla lain the operation of sign	in the operation of a	Colpitt's oscillator. ed amplifier and dra	w its frequency response. (08 Marks)
6	a.	Cho	For a differential am	plifier $A_d = 10000$ a	nd CMRR = 10^8 . W	(04 Marks) hat is the value of A _c ?
		ii)	A) = 10^{-4} For an inverting op—	B) 10^{-6} amp if $R_1 = R_F$ then	C) 10 ⁴ circuit is called	D) 100
	A) Sign changer B) Sign multiplier C) +ve sign D) N iii) The ideal bandwidth of an op-amp is				D) None of these	
		iv)	A) Zero Buffer and level shif	B) Infinity ter is usually a	C) High	D) Medium
		11)	A) Current follower		B) Collector fol	llower
	C) Resistance follower D) Emitter follower					ower
 b. Define the following terms with respect to op-amps i) Slew rate ii) Power supply rejection ratio iii) CMRR. c. Derive the expression of output voltage of a op-amp differentiator. d. Determine the output voltage for the op-amp adder circuit shown in Fig. Q.6(compared to the compared to the com						') (') ('DD) (0('M', h-)
						,
						in Fig. Q.6(d). (05 Marks)
						in 11g. Q.o(u). (00 Maria)
				IKA	1444	
			47	0-M	1	
			- 2.V	0-ML 2K2 0-ML	-	_ ~ 4.4
				•	+	oΛ ^o
			47			
				3K1 -	느	
				Fig. 6	Q.6(d)	
7	a.	Cho	oose the correct answe	rs for the following	:	(04 Marks)
		i)	The carrier frequence	y is mo	dulating frequency	
			A) Lower than		C) Equal to	D) None of these
		ii)	The bandwidth of A		- (C) 6/2	D) None of these
		. :::5	A) 2fm	B) fm	C) fm/2	D) None of these
		`iii)	Find the decimal eq A) 3267	B) 4265	C) 4268	D) 4267
		iv)			•	
		**)	A) 001 001 010 110		B) 100 001 010	0 110
			C) 110 110 001 001		D) 001 001 110	
	b .	Dra	aw the block diagram	of superheterodyne	receiver and explain	the function of each block
• G					(08 Marks) (03 Marks)	
	c. Convert $(BCDE)_{16} = ()_2 = ()_8 = ()_{10}$. d. Subtract $(57)_{10}$ from $(43)_{10}$ using 2's complement from.				(05 Marks)	
					(33 3:===3)	

8	a.	Choose the correct answers for the following:				(04 Marks)	
		i)	For NAND- Gate both inputs are high, then output will be				
			A) High	B) Low	C) Tristate	D) None of these	
		ii)	$Y = \overline{AB} + AB$ is a Boolean expression for				
		·	A) EX – OR	B) EX - NAND	C) $EX - NOR$	D) None of these	
		iii)	A+(B+C) = (A+B)+C is a property				
			A) Associative	B) Commutative	C) Distributive	D) None of these	
		iv)	The expression $Y =$	implified is	·		
			A)B+C	B) AB	C) A + \overline{B}	D) AB+C	
	Ъ.	Simplify the following Boolean expressions					
		$Y = \overline{ABC} + \overline{ABC} + A\overline{BC} + A\overline{BC}$					
		Y =	$(A\overline{B} + \overline{A}C)(BC + B\overline{C})$	(ABC)		(06 Marks)	
	C.	Draw the logic circuit of a full adder and also write its truth table with sum and carry expressions. (06 Marks)					
	d.	Reali	ize the expression F =	$=\overline{(X+Y(\overline{Z}+\overline{Y})}$ using of	only NAND - Gates.	(04 Marks)	

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